Application No.: 09/416,959 Docket No.: 501.35437CV2

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 41. (Cancelled)

42. (Currently Amended) A semiconductor integrated circuit device having a first portion for a memory array and a second portion for a circuit other than the memory array on a semiconductor substrate comprising:

a MISFET arranged in said first portion, said MISFET having first semiconductor regions and a gate electrode between said first semiconductor regions;

second semiconductor regions arranged in said second portion;

a first insulating film formed over said semiconductor substrate to cover said first and second portions;

a plurality of first openings formed simultaneously in said first insulating film above both said first and second portions;

a plurality of first conductor plugs formed in said first openings in said first insulating film on said first semiconductor regions in said first portion and on said second semiconductor regions in said second portion;

a first conductive strip formed on said first insulating film in said first portion and electrically connected to one of the first semiconductor regions of said MISFET

through one of said first conductor plugs, wherein said first conductive strip is formed in a separate manufacturing step from said first conductor plugs; and

a second conductive strip formed on said first insulating film in said second portion and electrically connected to said second semiconductor regions through said first conductor plugs to electrically connect said second semiconductor regions to one another through said second conductive strip, wherein said second conductive strip is formed in a separate manufacturing step from said first conductor plugs;

insulative spacers formed at least over one of upper surfaces or sidewalls of said first and second conductive strips;

a second insulating film formed over said first insulating film and said first and second conductive strips;

a second opening formed in said second insulating film over an upper surface of one of the first conductor plugs formed in one of said first openings in the first insulating film and connected to the other of said first semiconductor regions of said MISFET;

a second conductor plug formed in said second opening in said second insulating film to electrically connect with said one of said first conductor plugs connected to the other of said first semiconductor regions of said MISFET; and

a third conductive strip formed on said second insulating film and electrically connected to said second conductor plug,

wherein one of first conductor plugs is directly physically connected to one of the first semiconductor regions and the first conductive strip in said first portion and another of the first conductor plugs is directly physically connected to one of the

second semiconductor regions and the second conductive strip in the second portion.

43. (Previously Presented) A semiconductor integrated circuit device according to claim 42, wherein each of said first conductor plugs comprises a tungsten film.

44. (Previously Presented) A semiconductor integrated circuit device according to claim 43, wherein each of said first conductor plugs comprises a multiplayer film of titanium nitride and tungsten.

45. (Previously Presented) A semiconductor integrated circuit device according to claim 43, wherein said second semiconductor regions comprise an n-type semiconductor region and a p-type semiconductor.

46. (Previously Presented) A semiconductor integrated circuit device according to claim 45, wherein said second conductor plug comprises a tungsten film.

47. (Currently Amended) A semiconductor integrated circuit device having a first portion for a memory array and a second portion for a circuit other than the memory array on a semiconductor substrate comprising:

a MISFET arranged in said first portion, said MISFET having first semiconductor regions of n-type conductivity and a gate electrode between said first semiconductor regions;

a second semiconductor region of n-type conductivity and a third semiconductor region of p-type conductivity arranged in said second portion;

a first insulating film formed over said semiconductor substrate to cover said first and second portions;

a plurality of first openings formed simultaneously in said first insulating film above both said first and second portions;

a plurality of first conductor plugs each comprising a tungsten film formed in said first openings in said first insulating film on said first semiconductor regions in said first portion and on said second semiconductor regions in said second portion;

a first conductive strip formed on said first insulating film in said first portion and electrically connected to one of the first semiconductor regions of said MISFET through one of said first conductor plugs, wherein said first conductive strip is formed in a separate manufacturing step from said first conductor plugs; and

a second conductive strip formed on said first insulating film in said second portion and electrically connected to said second and third semiconductor regions through said first conductor plugs to electrically connect said second and third semiconductor regions to one another through said second conductive strip, wherein said second conductive strip is formed in a separate manufacturing step from said first conductor plugs;

<u>insulative spacers formed at least over one of upper surfaces or sidewalls of said first and second conductive strips;</u>

a second insulating film formed over said first insulating film and said first and second conductive strips;

a second opening formed in said second insulating film over an upper surface of one of the first conductor plugs formed in one of said first openings in the first insulating film and connected to the other of said first semiconductor regions of said MISFET;

a second conductor plug formed in said second opening in said second insulating film to electrically connect with said one of said first conductor plugs connected to the other of said first semiconductor regions of said MISFET; and

a third conductive strip formed on said second insulating film and electrically connected to said second conductor plug,

wherein one of first conductor plugs is directly physically connected to one of the first semiconductor regions and the first conductive strip in said first portion and another of the first conductor plugs is directly physically connected to one of the second semiconductor regions and the second conductive strip in the second portion.

48. (Previously Presented) A semiconductor integrated circuit device according to claim 47, wherein each of said first conductor plugs comprises a multi-layer film of titanium nitride and tungsten.

49. (Previously Presented) A semiconductor integrated device according to claim 47, wherein said second conductor plug comprises a tungsten film.

50. (Previously Presented) The semiconductor integrated device according to claim 42, further comprising:

first silicide layers formed between surfaces of said first semiconductor regions and said plurality of first conductor plugs formed in said openings in said first insulating film on said first semiconductor regions; and

second silicide layers formed between surfaces of said second semiconductor regions and said plurality of first conductor plugs formed in said openings in said first insulating film on said second semiconductor regions.

51. (Previously Presented) The semiconductor device according to claim 47, further comprising:

first silicide layers formed between surfaces of said first semiconductor regions and said plurality of first conductor plugs formed in said openings in said first insulating film on said first semiconductor regions; and

second silicide layers formed between surfaces of said second semiconductor regions and said plurality of first conductor plugs formed in said openings in said first insulating film on said second semiconductor regions.